

## **What is claimed is:**

**[Claim 1] 1. An electrostatic discharge (ESD) protection circuit formed on a P-type substrate comprising:**

- a first power terminal;
- a second power terminal;
- a resistor connected to the first power terminal;
- a capacitor connected between the resistor and the second power terminal;
- a first  $p^+$  diffusion region in the P-type substrate connected to the second power terminal;
- an N-well in the P-type substrate;
- a first  $n^+$  diffusion region in the N-well connected to the first power terminal;
- a P-well in the N-well;
- at least a second  $p^+$  diffusion region in the P-well, at least a second  $n^+$  diffusion region in the P-well connected to the first power terminal, and at least third  $n^+$  diffusion region in the P-well connected to the second power terminal; and
- an ESD detecting circuit connected to the first power terminal having an input terminal connected to the resistor and the capacitor and a output terminal connected to the second  $p^+$  diffusion region, wherein the output terminal outputs signal opposite to signal received by the input terminal so as to change a voltage level of the P-well.

**[Claim 2] 2. The ESD protection circuit of claim 1, wherein when a positive pulse is applied to the first power terminal, a PN junction is formed between the P-well and the third  $n^+$  diffusion region.**

**[Claim 3] 3. The ESD protection circuit of claim 1, wherein there is at least an NMOS transistor in the P-well, a drain of the NMOS transistor is the second  $n^+$  diffusion region, a source of the NMOS transistor is the third  $n^+$  diffusion region, and a body of the NMOS transistor is the P-well.**

**[Claim 4] 4. The ESD protection circuit of claim 3, wherein a gate of the NMOS transistor is connected to the second power terminal.**

**[Claim 5]** 5. The ESD protection circuit of claim 3, wherein a gate of the NMOS transistor is connected to the output terminal of the ESD detecting circuit.

**[Claim 6]** 6. The ESD protection circuit of claim 1, wherein an n-p-n bipolar junction transistor (BJT) is formed in the P-well, a collector of the BJT is the second n<sup>+</sup> diffusion region, a base of the BJT is the P-well, and an emitter of the BJT is the third n<sup>+</sup> diffusion region.

**[Claim 7]** 7. The ESD protection circuit of claim 1, wherein the ESD detecting circuit is an inverter.

**[Claim 8]** 8. The ESD protection circuit of claim 1, wherein the ESD detecting circuit is a PMOS transistor.

**[Claim 9]** 9. The ESD protection circuit of claim 1, wherein the second p<sup>+</sup> diffusion region is positioned between two of the second n<sup>+</sup> diffusion regions.

**[Claim 10]** 10. The ESD protection circuit of claim 1, wherein the second n<sup>+</sup> diffusion region and the third n<sup>+</sup> diffusion region are surrounded by the second p<sup>+</sup> diffusion region.

**[Claim 11]** 11. An electrostatic discharge (ESD) protection circuit formed on a P-type substrate comprising:

- a first p<sup>+</sup> diffusion region in the P-type substrate;
- an N-well in the P-type substrate;
- a first n<sup>+</sup> diffusion region in the N-well;
- a P-well in the N-well; and
- an n-p-n bipolar junction transistor (BJT) formed in the P-well, wherein an equivalent circuit between a base and an emitter of the BJT is a diode without connecting to any resistor in parallel.

**[Claim 12]** 12. The ESD protection circuit of claim 11 further comprising:

- a first power terminal connected to the first n<sup>+</sup> diffusion region;
- a second power terminal connected to the first p<sup>+</sup> diffusion region;

a resistor connected to the first power terminal;  
a capacitor connected between the resistor and the second power terminal;  
at least a second  $p^+$  diffusion region in the P-well, at least a second  $n^+$  diffusion region in the P-well connected to the first power terminal, and at least third  $n^+$  diffusion region in the P-well connected to the second power terminal; and  
an ESD detecting circuit connected to the first power terminal having an input terminal connected to the resistor and the capacitor and a output terminal connected to the second  $p^+$  diffusion region, wherein the output terminal outputs signal opposite to signal received by the input terminal so as to change a voltage level of the P-well.

**[Claim 13] 13.** The ESD protection circuit of claim 12, wherein there is at least an NMOS transistor formed in the P-well, a drain of the NMOS transistor is the second  $n^+$  diffusion region, a source of the NMOS transistor is the third  $n^+$  diffusion region, and a body of the NMOS transistor is the P-well, the n-p-n BJT is a parasitic lateral bipolar junction transistor of the NMOS transistor.

**[Claim 14] 14.** The ESD protection circuit of claim 13, wherein a gate of the NMOS transistor is connected to the second power terminal.

**[Claim 15] 15.** The ESD protection circuit of claim 13, wherein a gate of the NMOS transistor is connected to the output terminal of the ESD detecting circuit.

**[Claim 16] 16.** The ESD protection circuit of claim 12, wherein a collector of the BJT is the second  $n^+$  diffusion region, a base of the BJT is the P-well, and a emitter of the BJT is the third  $n^+$  diffusion region.

**[Claim 17] 17.** The ESD protection circuit of claim 12, wherein the ESD detecting circuit is an inverter.

**[Claim 18] 18.** The ESD protection circuit of claim 12, wherein the ESD detecting circuit is a PMOS transistor.

**[Claim 19]** 19. The ESD protection circuit of claim 12, wherein the second p<sup>+</sup> diffusion region is positioned between two of the second n<sup>+</sup> diffusion regions.

**[Claim 20]** 20. The ESD protection circuit of claim 12, wherein the second n<sup>+</sup> diffusion region and the third n<sup>+</sup> diffusion region are surrounded by the second p<sup>+</sup> diffusion region.